In the Claims:

Please amend claims 1, 4, 11, 12, 14, 15, and 18. The claims are as follows:

1. (Currently amended) A method for defect diagnosis of a circuit design, the method comprising the steps of:

(a) identifying M design structures and N physical characteristics of the circuit design,

wherein M and N are positive integers,

wherein each design structure of the M design structures is testable as to pass or fail, and

wherein each physical characteristic of the N physical characteristics is present in at least one design structure of the M design structures;

(b) for each design structure of the M design structures of the circuit design, determining a fail rate and determining whether the fail rate is high or low; and

(c) if every design structure of the M design structures in which a physical characteristic of the N physical characteristics is present has a high fail rate, then flagging the physical characteristic as containing ~~being likely to contain~~ at least a defect.

2. (Original) The method of claim 1, wherein each of the M design structures comprises a design circuit selected from the group consisting of a design scan chain, a design memory cell, and a design macro.

3. (Original) The method of claim 2, wherein each of the M design structures comprises a design scan chain.

4. (Currently amended) The method of claim 1, further comprising the step of, if at least one design structure of the M design structures in which a physical characteristic is present has a low fail rate, then determining that the physical characteristic should not be flagged as containing ~~being likely to contain~~ at least a defect.

5. (Original) The method of claim 1, further comprising the step of delayering and inspecting a structure with the flagged physical characteristic for defects.

6. (Original) The method of claim 1, wherein the step of determining the fail rate for each design structure of the M structures of the circuit design comprises the steps of:

providing P circuits of the design structure, wherein P is a positive integer, and wherein P is selected independently for each design structure of the M design structures.

testing each circuit of the P circuits so as to determine whether each circuit passes or fails so as to determine the number of failing circuits of the P circuits; and

determining the fail rate of the design structure from P and the number of failing circuits of the P circuits from said testing.

7. (Original) The method of claim 6, wherein P is a same number for all M design structures.

8. (Original) The method of claim 7, wherein for each design structure of the M design structures, the P circuits of the design structure reside in a corresponding set of P identical chips for all the M design structures.

9. (Original) The method of claim 1, wherein the step of determining whether the fail rate is high or low comprises the step of determining that the design structure has a high fail rate if the fail rate of the design structure equals or exceeds an independently pre-specified threshold fail rate.

10. (Original) The method of claim 1, wherein the step of determining whether the fail rate is high or low comprises the step of determining that the design structure has a low fail rate if the fail rate of the design structure is less than an independently pre-specified threshold fail rate.

11. (Currently amended) A method for defect diagnosis of a circuit design, the method comprising the steps of:

(a) identifying M design structures and N physical characteristics of the circuit design,

wherein M and N are positive integers,

wherein each design structure of the M design structures is testable as to pass or fail, and

wherein each physical characteristic of the N physical characteristics is present in at least one design structure of the M design structures;

(b) determining a fail rate for each design structure of the M design structures of the circuit design; and

(c) analyzing the fail rates of a plurality of design structures of the M design structures so as to determine whether to flag the physical characteristic as containing ~~being likely to contain~~ at least a defect.

12. (Currently amended) The method of claim 11, wherein the step of analyzing the fail rates comprises the steps of:

for each fail rate of a design structure of the M design structures, determining whether the fail rate is high or low; and

if every design structure of the M design structures in which the physical characteristic of the N physical characteristics is present has a high fail rate, flagging the physical characteristic as containing ~~being likely to contain~~ at least a defect.

13. (Original) The method of claim 11, wherein the step of identifying the M design structures and the N physical characteristics of the circuit design comprises the step of:

providing circuit design data and netlist for the circuit design; and

using software to process the circuit design data and netlist so as to identify the M design structures and the N physical characteristics of the circuit design.

14. (Currently amended) The method of claim 13, wherein the step of analyzing the fail rates comprises the steps of:

for each fail rate of a design structure of the M design structures, determining whether the fail rate is high or low; and

if all physical characteristics present in a first design structure are also present in a second design structure, except for a present physical characteristic[[s]] which is ~~id~~ present in the first design structure but not in the second design structure, and if the first design structure has a high fail rate and the second design structure has a low fail rate, then flagging the present physical characteristic as containing ~~being likely to contain at~~ least a defect.

15. (Currently amended) A computer program product, comprising a computer usable medium having a computer readable program code embodied therein, said computer readable program code comprising an algorithm adapted to implement a method for analyzing defects of a circuit design, wherein a fail rate for each of a plurality of design structures is provided, said method comprising the steps of:

(a) identifying M design structures from the plurality of design structures and N physical characteristics of the circuit design,

wherein M and N are positive integers, and

wherein each physical characteristic of the N physical characteristics is present in at least one design structure of the M design structures;

(b) for each design structure of the M design structures of the circuit design, determining whether the fail rate of the design structure is high or low; and

(c) if every design structure of the M design structures in which a physical characteristic of the N physical characteristics is present has a high fail rate, then flagging the physical characteristic as containing ~~being likely to contain~~ at least a defect.

16. (Original) The computer program product of claim 15, wherein each of the M design structures comprises a design circuit selected from the group consisting of a design scan chain, a design memory cell, and a design macro.

17. (Original) The computer program product of claim 15, wherein each of the M design structures comprises a design scan chain.

18. (Currently amended) The computer program product of claim 15, wherein the method further comprises the step of, if at least one design structure of the M design structures in which a physical characteristic is present has a low fail rate, then determining that the physical characteristic should not be flagged as containing ~~being likely to contain~~ at least a defect.

19. (Original) The computer program product of claim 15, wherein the step of determining whether the fail rate of the design structure is high or low comprises the step of determining that the design structure has a high fail rate if the fail rate of the design structure equals or exceeds an independently pre-specified threshold fail rate.

20. (Original) The computer program product of claim 15, wherein the step of determining whether the fail rate of the design structure is high or low comprises the step of determining that the design structure has a low fail rate if the fail rate of the design structure is less than an independently pre-specified threshold fail rate.